AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information representing correspondence between logical state transitions at each input terminal of said at least one circuit and logical state transitions at each output terminal of said at least one circuit, and said delay information for said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of each path of the logic circuit that comprises ~~comprising~~ said at least one circuit, a delay time is selected from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the ~~last~~ input terminal whose logical transition finally triggered said low state to high state transition of ~~to transition from a low state to a high state that causes~~ said selected output terminal ~~to transition from a low state to a high state~~ according to the logical operation

information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the ~~first~~ input terminal whose logical transition finally triggered said high state to low state transition of ~~to transition from a high state to a low state that causes~~ said selected output terminal ~~to transition from a high state to a low state~~ according to the logical operation information.

2. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for each ~~at least one~~ of said plurality of circuits, said library further comprises logical operation information representing correspondence between logical state transitions at each input terminal ~~of said at least one circuit~~ and logical state transitions at each output terminal for each ~~of said at least one~~ circuit of said plurality of circuits, and said delay information for said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of a logic circuit that comprises circuits from said plurality of circuits, a delay time of each path between a plurality of input terminals and a selected output terminal of said at least one circuit is selected from said delay time information, wherein if said selected output terminal transitions from a low state to a high state, said delay time is selected based on the ~~last~~ input terminal of said plurality of input terminals whose logical transition

finally triggered said low state to high state transition of ~~to transition from a low state to a high state that causes~~ said selected output terminal ~~to transition from a low state to a high state~~ according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on the ~~first~~ input terminal of said plurality of input terminals whose logical transition finally triggered said high state to low state transition of ~~to transition from a high state to a low state that causes~~ said selected output terminal ~~to transition from a high state to a low state~~ according to the logical operation information.

3. (*Currently Amended*) A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal for ~~of~~ at least one circuit of said plurality of circuits, said delay information for said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals as represented by said logical operation information for said at least one circuit; and

if the logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the ~~last~~ input terminal whose logical transition finally triggered said low state to high state transition of ~~to~~

~~transition from a low state to a high state that causes~~ said selected output terminal ~~to transition from a low state to a high state~~ according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the ~~first~~ input terminal whose logical transition finally triggered said high state to low state transition of ~~to transition from a high state to a low state that causes~~ said selected output terminal ~~to transition from a high state to a low state~~ according to the logical operation information.

4. (*Currently Amended*) A computer-readable medium having stored thereon a program for executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

~~a process step comprising:~~

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of each one of said plurality of circuits, said delay information for ~~said~~ at least one circuit of said plurality of circuits is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals as represented by said logical operation information for said at least one circuit; ~~and~~

if said ~~a~~ logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the ~~last~~

input terminal whose logical transition finally triggered said low state to high state transition of ~~to transition from a low state to a high state that causes~~ said selected output terminal ~~to transition from a low state to a high state~~ according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the ~~first~~ input terminal whose logical transition finally triggered said high state to low state transition of ~~to transition from a high state to a low state that causes~~ said selected output terminal ~~to transition from a high state to a low state~~ according to the logical operation information; and

~~a process step of~~ performing a delay calculation to determine a propagation delay time using said selected delay time ~~as a propagation delay time~~ of said at least one circuit.